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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,848	10/30/2003	Christopher D. S. Donham	019680-003300US	8095

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EXAMINER	
TUNG, KEE M	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,848	DONHAM ET AL.	
	Examiner	Art Unit	
	Kee M. Tung	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *39-45* is/are allowed.

6)☒ Claim(s) *28-36,38 and 46-54* is/are rejected.

7)☒ Claim(s) *37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election/amendment of claims 28-37 (by canceled claims 1-27) in the reply filed on 7/20/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election/amendment has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 112

2. Claim 29 recites the limitation "the external memory" in line 2. There is insufficient antecedent basis for this limitation in the claim.

3. Claim 30 recites the limitation "the graphics memory" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 28-36, 38, and 46-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omtzigt (6,067,643) in view of Van Hook et al (6,239,810 hereinafter "Van") and Saito et al (6,940,519 hereinafter "Saito").

Omtzigt teaches a graphics processor (Fig. 1, 152 and 154) comprising a shader circuit (color pipe 230, col. 4, lines 23-26); a texture circuit (240) coupled to the shader circuit; and a frame buffer interface (memory I/F 260) coupled to the texture circuit, wherein the texture circuit retrieves a plurality of textures from an external memory (158) coupled to the frame buffer interface and textures are stored in the texture cache (244). However, Omtzigt fails to explicitly teach or suggest "texture descriptors". This is what Van teaches. Van teaches a texture memory (502) for storing texture descriptors (Fig. 22, col. 50, lines 15-49). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of coprocessor 200 comprising a display processor 500 having a texture memory (502) stores texture descriptors of Van into the system of Omtzigt because texture descriptor provides information about the texture as taught by Van (col. 50, lines 37-49) and thus provides better texture mapping processing. However, the combined system still fails to teach or suggest the texture descriptors are stored in the texture memory externally and retrieve via the frame buffer interface. Saito teaches a video memory (Fig. 4, 13) comprising a texture memory (30); frame buffer (31). Accessing to the video memory by the GPU (8) (12) via a memory I/F circuit (11). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Saito into the combined system of Omtzigt and Van in order to more efficiently use of the graphics memory by shared the texture memory with the display buffer and further avoid the possibility of extra (unused) memory. Therefore, at least claim 31 would have been obvious.

Claim 28 is similar in scope to claim 31, and additionally requires the graphics processor is an integrated circuit. Saito teaches the GPU is an integrated circuit (Fig. 26A, and col. 17, lines 51-53).

As per claim 29, the combined system teaches the texture circuit retrieves texture descriptors (Van, 502) from the external memory (Ozawa, 16) using the frame buffer interface (Ozawa, 13).

As per claim 30, Saito teaches the shader (21) provides an instruction for texture circuit to retrieve the texture descriptors from the graphics memory (13).

As per claims 32-35, the combined system fails to explicitly teach or suggest the texture descriptor identified by an address, a pointer and/or an index. However, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to that data (texture descriptors) stored in the memory is normally identified by an address, or pointer (such as, in a FIFO type) or index in order to more efficiently and effectively access (read or write) the memory. Therefore, at least claims 32-35 would have been obvious.

Claim 36 is similar in scope to claim 31, and additionally requires the shader (21) requests texture descriptors from the frame buffer interface (11).

As per claim 38, Van teaches at least one of the plurality of texture descriptors is retrieved a plurality of times (it was old and well known in the art that data stored in the memory can be retrieved in multiple times).

As per claim 46, the claim 46 is similar in scope to claim 31, and additionally requires the shader circuit (21) is configured to instruct the frame buffer interface (11) to

retrieve a first texture descriptor, and the texture circuit (Omtzigt, 240) is configured to receive a first texture from the frame buffer interface (260), the first texture identified by the first texture descriptor (Van, 502).

As per claim 47, Omtzigt teaches a texture cache (244) configured to store the first texture.

As per claim 48, Omtzigt teaches a texture filter (texture pipe 240 performs texture filter function) configured to filter the first texture.

Claims 49 and 50 are similar in scope to claim 38, and thus are rejected under similar rationale.

As per claims 51-54, the combined system fails to explicitly teach or suggest the texture descriptor identified by an address, a pointer and/or an index. However, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to that data (texture descriptors) stored in the memory is normally identified by an address, or pointer (such as, in a FIFO type) or index in order to more efficiently and effectively access (read or write) the memory. Therefore, at least claims 51-54 would have been obvious.

Specification

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The title says a "method", however, there is no "method" being claimed.

Allowable Subject Matter

7. Claims 39-45 are allowed.

8. Claim 37 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: The prior art made of record fails to anticipate or make obvious the claimed subject matter. Specifically, the prior art fails to teach or suggest, in combination with the remaining elements, an integrated circuit comprising a texture descriptor cache controller as recited in claim 37; the shader circuit is configured to receive a first texture descriptor, a first hint, and a first command ...., as recited in claim 39; and the shader circuit is configured to receive a portion of a shader program includes a first command ...., as recited in claim 44.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M. Tung whose telephone number is 571-272-7794. The examiner can normally be reached on Tuesday - Friday from 5:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kee M Tung
Primary Examiner
Art Unit 2671